REMARKS

The specification has been reviewed without identifying any minor errors that need correcting.

The examiner rejected claims 1-3, 5-10 and 12 under 35 U.S.C. §103(a) over Cherukuri, U.S. Patent No. 6,006,307 in view of Rusu et al, U.S. Patent No. 6,137,807. Claims 4 and 11 stand rejected over the '307 and '807 patents and further in view of Kawaguchi et al., U.S. Publication No. 2001/0030900 A1.

Regarding claims 1 and 6, the examiner states that Cherukuri teaches a method of memory management comprising:

providing multiple banks of memory devices organized into independent channels wherein each bank of memory devices contains duplicate data;

providing a tree memory controller for controlling data read and write accesses to each of the banks in each of the channels;

sending read or write requests to the tree memory controller; and

establishing a bank queue for each bank in each channel.

The examiner then states that Cherukuri does not teach that a bank queue for each bank designates bank availability; checking at the tree memory controller, the availability of each bank; identifying a first available bank; and executing the read request from the first available bank.

As the examiner has recognized, Cherukuri does not teach that a bank queue is established for each bank to designate bank availability. However, it should also be noted that Cherukuri does not establish queues for both read and write operations. The discussion at column 6, line 63 et seq. for Cherukuri only discusses the use of a queue when a write command is issued during the time that a pre-fetch operation is occurring. There is no indication that Cherukuri considers using a queue during a read operation.

The patent to Rusu et al. describes a more common type of queuing system in which data can be stored into one of two or more memory banks depending upon which memory bank is available at the time that the data input is

received. It should be noted that Rusu does not have a mirrored memory system and is not concerned with the same types or problems that applicant is dealing with in a mirrored memory system. While there are some surface similarities between the elements cited by the examiner in Rusu and the same types of elements in applicant's specification, the uses and functions of those elements are entirely different since applicant is dealing with duplicating or mirroring data in two or more memory banks while Rusu is only concerned with storing data into a single one of a plurality of memory banks. As noted in column 4, lines 40-45 of Rusu, the memory management program used by Rusu allows concurrent reading and writing to memory, i.e., one of the banks can be read while data is being written to another of the banks. This operation is completely different from the operation of applicant's system in which the identical data is stored in all memory banks and a write operation writes to each memory bank concurrently thereby preventing concurrent reading and writing.

Based upon the description set forth in Rusu et al, the examiner's comments regarding the use of the bank queue for designating bank availability for a read request would not make logical sense. If a particular piece of data were needed, the controller could not select a particular memory bank since the data that is requested would only be stored in one of the memory banks. Accordingly, it is not seen how Rusu would suggest that the dual memory system such as that used in Cherukuri could be modified so that a read operation from memory would require a test of bank availability. Rusu et al. would not be concerned with the bank availability issue if the same data were written to both memory banks. Accordingly, it is not seen how it would be obvious to use the bank availability system in Rusu et al. in the Cherukuri application. More specifically, the Cherukuri and Rusu et al. patents disclose entirely different types of systems and a programmer or system designer would not be led from one to the other because of those differences in systems.

Still further, it is not seen how one would take the teachings of Rusu et al. and apply them to the system of Cherukuri. Rusu et al. is directed to a memory bank system which can do simultaneous or concurrent reading and writing by

utilizing two separate and independent memory banks. Cherukuri uses a mirrored memory system so that concurrent reading and writing is not possible. Accordingly, it is submitted that there is no teaching or suggestion in Cherukuri that would lead one to combine the teachings of Rusu et al. into the Cherukuri application.

As the examiner is well aware, the development of patent law has led to the holding on a routine basis that there must be some teaching or suggestion in the cited references that would lead one to make the proposed combination. The applicant's specification cannot be used as a road map to guide one to find these different combinations. In this instance, the only suggestion to implement applicant's claimed invention is applicant's specification. There is simply nothing in either Cherukuri or Rusu et al. that would suggest that one could take the teachings of one of those patents and combine it with the other. The teachings of those two patents are simply too far apart to allow one to make the leap from Cherukuri to Rusu et al. without some outside guidance that would suggest that elements of Rusu et al. could be utilized in the mirror memory system of Cherukuri. Without applicant's specification, there would be no such suggestion. Accordingly, it is submitted that the rejection based upon the combination of Cherukuri and Rusu et al. is improper and should be withdrawn.

Turning now to the rejection of claim 2, the examiner states that Cherukuri teaches that the step of executing for a write access includes blocking all read requests, citing column 5, line 26 of Cherukuri. Applicant's attorney is not sure whether this citation is correct since that particular sentence relates to the ability of the microprocessor to limit fetch operations performed via a pre-fetched channel to read operations only. While Cherukuri describes a mirrored memory system, it should be noted that the storage of data in memory occurs by first reading the memory to memory bank 20a and then transferring from 20a to memory bank 20b. In other words, there is no concurrent writing to both memory banks. However, Cherukuri does have the ability to concurrently read from different memory banks via either the fetched channel or the pre-fetched

channel. Thus, there are other significant differences between the operation of Cherukuri and applicant's claimed invention.

Continuing with claim 2, the examiner also states that Cherukuri confirms a data to be written as complete for the selected memory word length citing column 5, lines 22-24. Applicant's attorney has read and re-read that section of the Cherukuri patent and is unable to find a statement that supports the examiner's position. The examiner further states that at column 6, lines 63 to column 7, lines 14, Cherukuri teaches waiting for each bank queue to indicate bank availability for all banks concurrently. It is also not believed that Cherukuri performs this function. Note that at column 7, beginning at line 5, Cherukuri specifically points out that memory bank 20a is coupled to fetch channel 16 and does not require a write queue. Accordingly, there is no indication that bank availability for all banks concurrently need be determined.

The examiner's comments regarding claims 3 and 5 appear to be correct. Regarding claim 7, however, Cherukuri does not describe at column 5, lines 22-26 that the controller suspends all read requests during processing of a write request. The discussion at the cited location of Cherukuri only describes a possible operation and suggests that one microprocessor may limit the fetch operations performed via a pre-fetched channel to read operations. It is not seen how this constitutes suspension of all read requests during processing of a write request.

The examiner's comments regarding claims 8, 9, 10 and 12 appear to be supported by the Cherukuri description. However, it appears that there may be more than one embodiment in Cherukuri and is not clear at column 4 whether the concurrent writing to the first and second memory banks is mandatory or merely an opportunistic event.

Turning now to the rejection of claims 4 and 11, the examiner has rejected these claims under 35 USC §103(a) as being unpatentable over Cherukuri and Rusu et al. and further in view of Kawaguchi. It appears that Kawaguchi is cited merely because Kawaguchi uses FCRAM for semiconnector memory. It is noted that applicants' are not claiming that they are the inventors of FCRAM but

merely that FCRAM devices are utilized as preferred memory devices in one embodiment of applicants' invention. It is not seen that it would be obvious to utilize FCRAM in applicants' claimed invention merely by the fact that such devices exist as shown by Kawaguchi. There is nothing in Kawaguchi that suggests the use of FCRAM in a system as taught by applicant. Further, as pointed out above, the combination of Cherukuri and Rusu et al. does not teach nor suggest applicants' claimed invention and the combination of Kawaguchi does nothing to further that teaching. Accordingly, the rejection of claims 4 and 11 over the combination of Cherukuri, Rusu et al. and Kawaguchi et al. should be withdrawn.

Claim 13 stands rejected under 35 USC §103(a) over Cherukuri, Rusu et al. and further in view of Bouchard et al. For the reasons set forth above, it is submitted that there is no teaching or suggestion in Cherukuri and Rusu et al. to make the combination that is the basis of claim 6 from which claim 13 depends. Accordingly, it is submitted that claim 13 is distinguishable over the cited art for the reasons set forth above in the discussion of Cherukuri and Rusu et al.

For all the reasons set forth above, it is submitted that the patents to Cherukuri and Rusu et al. taken alone or in combination do not teach the invention as set forth in applicants' claims and that all the claims presently pending in the application are patentably distinguishable over the cited references. Reconsideration of the rejection of claims 1-13 is therefore requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I HEREBY CERTIFY that this Request For Reconsideration is being mailed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 26th day of January, 2004.

Shirley Goff